REMARKS

The Examiner's Office Action of April 5, 2006 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application, and for indicating claims 11 and 12 as containing allowable subject matter and would be allowed if rewritten to include all of the limitation of the base claim and any intervening claims.

Claims 1-12 were pending prior to the instant amendment. By this amendment, claims 1, 5, 6, 8, 10 and 12 have been amended. New claims 13 and 14 have been added. Accordingly, claims 1-14 are pending, of which claim 1 is independent.

In the detailed Office Action, claims 1-4 and 10 stand rejected under 35 U.S.C. §102(b) as being anticipated by Takeshi et al. (JP 5026923 – hereafter Takeshi). Further, claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Tamura et al. (U.S. Patent No. 6,707,727 – hereafter Tamura) in view of Cao et al. (U.S. Publication No. 2003/0001634 – hereafter Cao). Still further, claims 6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Takeshi in view of Kuwata (U.S. Patent No. 6,959,061 – hereafter Kuwata). Still further, claims 6, 8 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pan (U.S. Patent No. 6,348,823 – hereafter Pan) in view of Kuwata. Finally, claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Pan in view of Kuwata. These rejections are respectfully traversed at least for the reasons provided below.

Initially, amendments have been made in the claim language to improve the clarity and correct grammatical errors.

In addition, claim 1 has been amended by adding two limitations: (1) the selected clock signal and a second clock signal are supplied to a central processing unit, and (2) the frequency of the second clock signal differs from the frequency of the first clock signal and the selected clock signal.

Accordingly, amended claim 1 provides a central processing unit (CPU) with two clock signals having different frequencies and a predetermined phase relationship, as discussed in the first sentence in the discussion of the related art on page 1 of the specification. The central processing unit is shown as element 3 in Fig. 1, for example.

With respect to Takeshi, according to the drawings cited by the Examiner in the rejection of claim 1, a phase adjustment circuit is show which receives two clock signals (1, 2) having the same frequency and outputs a third clock signal (6), which also has the same frequency. Further, Applicant respectfully note that the destination of the third clock signal is not disclose by Takeshi and that the specification is completely silent about supplying two clock signals with different frequencies to a central processing unit.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Takeshi, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-5 and 10, under 35 U.S.C. §102(b), as anticipated by Takeshi is improper.

The arguments and amendments discussed above in relation to the rejection of claim 1 are also applicable to its dependent claims, including claims 6 and 8 which are allegedly obvious over Takeshi and Cao.

With respect to the rejection of claim 5 over Tamura and Cao, Applicant respectfully notes that the Examiner appears to have not discussed how Tamura and Cao are relevant to the features recited in claim 1, from which claim 5 depends. That is, the Examiner merely addressed the features recited in claim 5. Therefore, without any indication of how Tamura and Cao are applicable to claim 1, Applicant cannot respond to the rejection. Further, Applicant respectfully assert that the above arguments in relation to the rejection of claim 1 over Takeshi are also applicable to the rejection of claim 5, and that Tamura and Cao appears to be deficient in teaching, disclosing or suggesting at least a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied, as recited in amended claim 1. Should the Examiner maintain the reject of claim 5 over Tamura and Cao, Applicant would respectfully request the Examiner to point out specific text and drawings in Tamura and Cao supporting Applicant's claimed features of claim 1.

With respect to the obviousness rejection of dependent claims 6-9 over Pan and Kuwata, the above-presented amendments and arguments in relation to the anticipatory rejection of claim 1 are also applicable. That is, Pan and Kuwata also fail to teach, disclose

or suggest a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied, as recited in amended claim 1.

New dependent claims 13 and 14 have been added to further complete the scope to which Applicant is entitled. New dependent claim 13 recites a phase adjustment circuit wherein the selected clock signal has a lower frequency than the second clock signal and the phase adjustment circuit operates to make rising and falling edges of the selected clock signal occur while the second clock signal is high. The features of this claim are supported by the description of the first embodiment and by Figs. 1 and 2, for example.

New dependent claim 14 recites a phase adjustment circuit wherein the selected clock signal has a higher frequency than the second clock signal and the phase adjustment circuit operates to make rising and falling edges of the second clock signal occur while the selected clock signal is high. This claim is supported by the description of the second embodiment and by Figs. 3 and 4, for example.

Applicant respectfully asserts that none of the cited references teach, disclose or suggests a phase adjustment circuit with the claimed features and operates as recited in new claim 13 or 14.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Takeshi, Tamura, Cao, Kuwata and Pan are deficient, as discussed above, their application, separately or combined, in the obviousness rejections is improper.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-14 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

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